

MULTI-JUNCTION CELLS WITH MONOLITHIC BYPASS DIODES

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ABSTRACT

Bypass diodes are attached electrically parallel (but with opposite polarity) to solar cells such that when the cells are reverse biased, the bypass diodes are forward biased, passing current and preventing the cells from going into reverse breakdown. For III-V single and multi-junction space cells, discrete silicon bypass diodes have typically been used. In this paper, we present a monolithic bypass diode, grown on top of the III-V solar cell. The bypass diode is of opposite polarity to the cell, but electrically parallel to the cell. The advantage of the monolithic diode over the discrete diode is the reduction in interconnects and handling required during the interconnecting of cells into strings. We present performance, reliability, and space qualification results for the monolithic bypass diode. Of particular importance are the diode reverse bias leakage current and the forward bias turn-on voltage. Large area ($\sim 30 \text{ cm}^2$) cell/monolithic diodes with efficiencies of 28% have been made.

1. INTRODUCTION

The manufacture of solar panels for both space and terrestrial applications involves stringing cells together such that they are connected electrically in series. If a solar cell in a series connected string is shaded, with the remaining cells still in the light, the cell is forced into reverse bias breakdown so that it can conduct the current of the string. The reverse biasing of the cell into breakdown can permanently damage the cell. For III-V single and multi-junction solar cells, discrete silicon bypass diodes have been electrically connected in parallel to the cell, but with opposite polarity, such that when the cell in the string is shaded, the bypass diode is forward biased and the current of the string is safely passed through the cell-bypass diode combination. The cell is prevented from being reverse biased into breakdown. Several different approaches to attaching a discrete diode to the solar cell have been proposed and are in use, including front mounted, corner mounted (in-plane with the cell), and back mounted diodes [1].

The connection of the discrete silicon diode to the cell is done during the CIC (coverglass-interconnect) operation, and involves front and back interconnects to both the diode and the cell. Automation of the CICing process is complicated because of the number of parts involved, i.e., by the cell, the diode, and the front and the back interconnects for the diode.

A monolithic bypass diode, integral to the solar cell and not a discrete part, has the advantage of reducing the number of parts required during the CICing operation. However, there are several design criteria that the

monolithic bypass diode must meet. First, it has to do its job. The monolithic bypass diode must perform the task of protecting the cell. Secondly, it has to be reliable. The diode has to be stable in a space environment, as well as perform repeatedly without failure. This will be discussed in later sections. Finally, it has to be simple. The inclusion of the diode must not add growth or processing complexity such that the reduction in CICing costs are outweighed by the monolithic diode's growth and processing costs.

We have looked at several different approaches to the monolithic bypass diode, including both Schottky and epitaxially grown p-n junctions. Both approaches have advantages and disadvantages, which will be discussed in the following sections.

2. DIODE DESIGN

The dark electrical schematic of the cell and diode is shown in Figure 1. As can be seen, the diode and the multi-junction cell are electrically parallel.

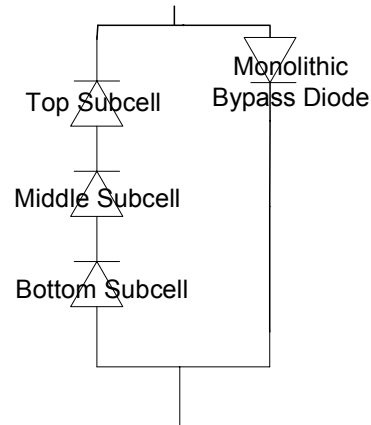


Fig. 1. Electrical schematic of the monolithic bypass diode, under dark conditions.

Figures 2 and 3 are schematics of the Schottky diode and epitaxial diode approaches, respectively. These schematics are not to scale, and the bypass diodes are actually much smaller in area compared to the cells that they are protecting. In terms of electrical performance, the key diode parameters are the reverse bias leakage current (I_{RB}) (measured at a value close to the cell load voltage, i.e., ~ 2.5 volts), the forward bias turn on voltage (V_{FB}) (approximately how much voltage is required to pass the load current), and the diode series resistance (R_S) (which is a measure of how much I^2R losses occur in the diode).

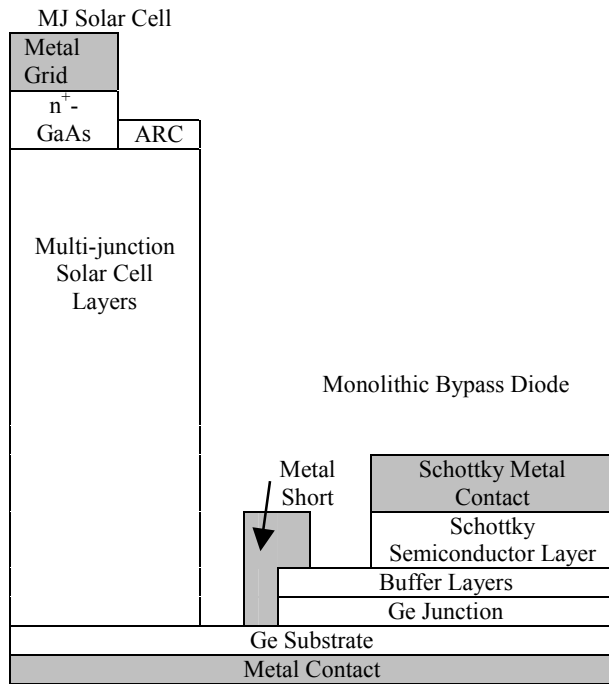


Fig. 3. Schematic of the Schottky diode approach. Note that neither the horizontal nor the vertical distances are to scale. The monolithic bypass diode area covers a much smaller portion of the cell (e.g., 7 mm^2 for the diode versus 30 cm^2 for the cell) than depicted here.

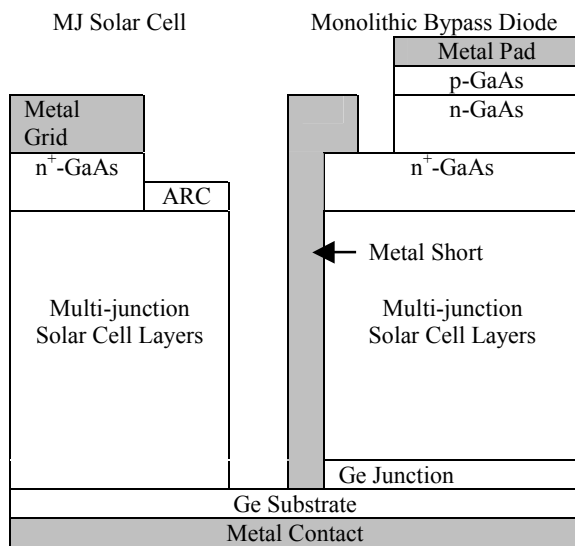


Fig. 3. Schematic of the p/n diode approach. The same comments regarding scales and areas mentioned for Figure 2 apply for this Figure.

2.1 Schottky Diode Approach

One of the advantages of the Schottky diode approach is that the diode can be located at any point in the structure. Since the junction is formed by the deposition of metal on a semiconductor, processing of the diode involves etching down to the appropriate semiconductor layer, and then depositing the appropriate metal necessary to make the junction. In Figure 2 the Schottky diode is placed in the buffer layers, above the Ge junction, but beneath the

epitaxially grown III-V layers. However, the Schottky diode could just as easily be placed on top of the III-V epitaxially grown layers. A mesa etch also has to be done to electrically isolate the diode area from the rest of the cell.

Figure 2 also shows “metal shorts”, necessary to short out the junctions underneath the Schottky diode. If these “metal shorts” are not included, the Schottky diode is in series with another diode underneath of opposite polarity. For the Schottky diode to protect the cell, the diode of opposite polarity has to be forced into reverse breakdown to allow the current to be conducted. The “metal short” resolves this issue by providing an electrical short around the opposite polarity diode underneath the Schottky diode. The “metal shorts” also remove the necessity of including welded straps or “C-clamps” for completing the electrical circuit. In both Figures 2 and 3 the circuit is completed through the interconnect tab (not shown). An interconnect tab welded to the top of the Schottky diode and the cell bus pads completes the circuit. Emcore has both US and international patents pending on the “metal shorts” approach.

One concern with the Schottky diode approach is the leakage current when the diode is in reverse bias. When the cell is operating in forward bias, i.e., at the load point, the bypass diode is reverse biased. Any leakage current going through the bypass diode directly reduces the total current through the cell/diode combination. Hence, the reverse bias leakage current through the Schottky diode needs to be kept to a minimum, ideally in the micro-amps range.

Low reverse bias leakage currents in Schottky diodes can be achieved two ways: reduced doping in the semiconductor layer, and increasing the bandgap of the semiconductor. Increasing the semiconductor bandgap increases the barrier height at the junction, hence decreasing the leakage current. It must be kept in mind that the semiconductor layer of the Schottky diode is also shared with the multi-junction cell. Decreasing the doping of the semiconductor layer is actually not an issue, as the current is conducted vertically through this layer, and the current density in the layer is relatively small. Using a higher bandgap semiconductor (i.e., GaInP_2 vs. GaAs) can actually be a larger issue since the appropriate gas switching must be done during metal-organic chemical vapor deposition (MOCVD) growth of the device. We have found that a low doped GaInP_2 layer actually works best in terms of leakage current. While requiring a higher turn on voltage in forward bias, the reduction in the diode reverse bias leakage current is an acceptable trade.

A major concern with the Schottky diode approach is that the actual junction occurs at the metal semiconductor interface. Schottky diodes are very dependent on the surface conditions of the semiconductor prior to deposition of the metal. This includes the thickness of any oxides that may have formed on the semiconductor surface, which is time dependent. Organic contaminants can also affect the barrier height at the metal/semiconductor junction. The variabilities in the semiconductor surface lead to a variability in the forward bias voltage required to turn on the diode, as well as the reverse bias leakage current.

Several other issues with the Schottky diode approach will be discussed in Section 2.3, Reverse Bias Breakdown, and again in Section 3, Diode Reliability.

2.2 P/N Junction Diode Approach

A schematic of the p/n diode approach is shown in Figure 3. In this approach the bypass diode is grown on top of the multi-junction cell. The complete diode is epitaxially grown, and is of opposite polarity to the multi-junction device. The diode layers are removed from the areas above the multi-junction cell, and a mesa etch isolates the bypass diode area from the cell. As with the Schottky diode approach, a “metal shorts” approach is again used to short out the multi-junction cell layers underneath the bypass diode.

The p/n junction approach has several advantages over the Schottky approach, one of which is that the junction interface can be precisely controlled during MOCVD growth. The doping levels of the p- and n-layers are precisely controlled, and the junction is also made in a tightly controlled environment (purified H₂ in the MOCVD reactor). Hence, the manufacturing repeatability issues associated with the Schottky diode are avoided.

2.3 Reverse Bias Breakdown

Testing of the diodes in reverse bias indicates a considerable amount about the diode’s robustness. Because the bypass diode is in the reverse biased condition when the cell is at load (at approximately 2.3 volts), not only does the leakage current through the diode have to be minimal, it also has to be stable. Since these bypass diodes may operate for up to 15 to 20 years in space, there cannot be pre-mature failures.

As part of the design phase of developing a monolithic bypass diode, we have taken both the Schottky and p/n diodes into far reverse bias to determine what kind of breakdown mechanisms were involved, and how stable the breakdown is. We looked at two different types of p/n junctions, which we refer to as Design 1 and Design 2. Because of pending US and international patents, we cannot disclose the particular details of these designs.

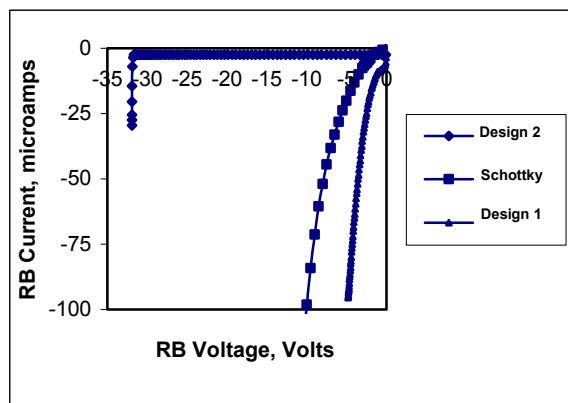


Fig. 4. Reverse bias I-V curves for Schottky, Design 1, and Design 2 monolithic bypass diodes. Note the qualitative difference between the Schottky and Design 1 diodes and the Design 2 diode. See text for further discussion.

The results of the reverse bias tests are shown in Figure 4. The vertical axis on the graph is in micro-amps. Testing the cells in reverse bias at these currents is a sensitive measure of the type of breakdown that is occurring. Note the qualitative difference between the breakdown characteristics between p/n diode Design 2 and the other two diodes, the Schottky diode and p/n diode Design 1. Design 2 shows avalanche breakdown (note the

sharp I-V characteristic, as compared to Zener breakdown) [2], while Design 1 and the Schottky design show “microplasma” breakdown associated with crystalline imperfections [2]. In the case of Design 1 and the Schottky design, we have been able to see the current pulses associated with the microplasmas on a curve tracer. The reverse bias I-V curves for the Schottky and Design 1 diodes will literally “flicker” as the microplasmas turn on and off. Because of the association of the microplasmas with crystalline defects and ensuing concerns about device reliability, we decided that both the Schottky and Design 1 approaches were not robust enough for space applications. Instead, we have focused on the p/n Design 2 bypass diode, which we have found to be stable under reverse bias conditions.

The ability of Design 2 to withstand a much higher reverse bias is also obvious in Figure 4. Typically, reverse biases of >30 volts prior to the onset of avalanche breakdown are seen. This is compared with the less than 5-10 volts that the Schottky and Design 1 diodes can withstand before the reverse bias leakage current is larger than 30 micro-amps.

3. DIODE QUALIFICATION

In order to be incorporated into a cell for use in space, the monolithic bypass diode has to pass several qualification steps. These tests include a welding test, a reverse bias soak, a forward bias soak, a cycling test, and performance comparisons before and after exposure to particle radiation.

We have looked at two different areas for the monolithic bypass diode. One diode has an area of 7 mm², while the second has an area of 4 mm². Slightly different qualification tests (the forward bias soak and cycling test) were used on the different diode areas. We have completed the qualification tests for the 7 mm² diode, while the tests for the 4 mm² diode are still in process.

The welding test was of particular concern for the Schottky diode approach. Since the junction in the Schottky diode actually occurs at the metal semiconductor interface, any high temperature welding to the contact metal always had the possibility of altering that interface. We have found that the Schottky junction can be particularly sensitive to welds, with an increase in the reverse bias leakage current (I_{RB}) due to the welding. The p/n junctions, both Design 1 and 2, were much less sensitive to the welding process, and the comparison of the diode performance pre- and post-weld gave confidence that either of these two designs could be welded. As a matter of fact, one of the conditions for having an acceptable weld was making sure that there was no change in the I_{RB} before and after the weld process.

The reverse bias soak, the forward bias soak, and the cycling tests were all done at 120 °C. The reverse bias soak involved holding the diode at 2.5 volts reverse bias for 1,000 hours, and comparing the diode performance before and after the soak. Two separate tests were used for the forward bias soak, depending on the diode area. For the 7 mm² diode, the diode was forward biased until 500 mA passed through the diode, while for the 4 mm² diode, 650 mA was passed through the diode in forward bias. These different current levels reflect the different light generated current for different cell types where these diodes would be used. For the cycling test, the diodes

were switched between 2.5 volts reverse bias and either 500 mA or 650 mA (for the 7 mm² and 4 mm² diode areas, respectively) over 100,000 times. The dwells at each of the biases were 1 second, with an approximately 1 milli-second switching time.

The particle irradiation involved exposure to both 1 MeV electrons, and 10 MeV protons. For 1 MeV electrons, the diodes were exposed to a fluence of 1×10^{15} e/cm², while for 10 MeV protons, the diodes were exposed to a fluence of 1×10^{12} p/cm².

The results for the 7 mm² diode are shown in Table 1. As can be seen using a p/n Design 2 diode, all of the tests were passed. As mentioned previously, we are currently qualifying the 4 mm² diode. We have completed the reverse bias soak, the cycling test, and the radiation tests, and the results are similar to those shown in Table 1. The forward bias soak will be starting shortly.

Test Item	Requirement	Results	Status
Reverse Bias	$I_{RB} < 30 \mu A$ $\Delta V_{FB} < 10\%$	$I_{RB} < 1 \mu A$ $\Delta V_{FB} = 1.6\%$	Pass
Forward Bias	$I_{RB} < 30 \mu A$ $\Delta V_{FB} < 10\%$	$I_{RB} < 1 \mu A$ $\Delta V_{FB} = 1.4\%$	Pass
Diode Cycling	$I_{RB} < 30 \mu A$ $\Delta V_{FB} < 10\%$	$I_{RB} < 1 \mu A$ $\Delta V_{FB} = 3.5\%$	Pass
Irradiation: Electrons Protons	$I_{RB} < 30 \mu A$ $\Delta V_{FB} < 10\%$	Electrons: $I_{RB} < 1 \mu A$ $\Delta V_{FB} < 1\%$ Protons: $I_{RB} < 1 \mu A$ $\Delta V_{FB} < 1\%$	Pass

Table 1. Summary of space qualification tests on the monolithic bypass diode Design 2, with 7 mm² area. I_{RB} was measured at 2.5 volts reverse bias, and ΔV_{FB} refers to the change in the forward bias voltage needed to pass 500 mA through the diode before and after the particular test. See text for further discussion.

4. CELL PLUS DIODE PERFORMANCE

We have made a number of cells with the monolithic bypass diode. Figure 5 shows the I-V curve for one of these cells, along with the device performance parameters. Figure 6 shows a histogram of the performance of 2,000 large area (>30 cm²) devices. The average efficiency for this group of cells is 27.5% (135.3 mW/cm²)

5. CONCLUSIONS

We have been able to demonstrate a monolithic bypass diode that meets the design criteria mentioned in Section 2. The diode performs as intended as it prevents the cell from being reverse biased into breakdown. It is robust and reliable, as demonstrated by the qualifications tests. Finally, it is simple in design and does not add significant complexity during growth and processing.

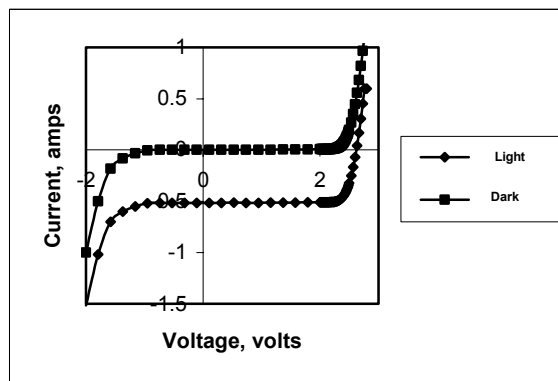


Fig. 5. I-V curve for a 30.2 cm² multi-junction solar cell with a Design 2 monolithic bypass diode. The cell Voc, Isc, ff, and efficiency are 2621 mV, 517 mA, 84.5%, and 28%, respectively, under 135.3 mW/cm².

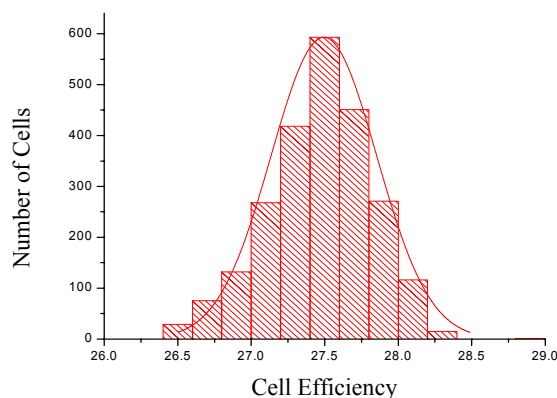


Fig. 6. Histogram for over 2,000 multi-junction cells grown with monolithic bypass diodes. All of these cells were 30 cm² in area or larger. The average efficiency is 27.5%, under 135.3 mW/cm².

REFERENCES

- [1] See, for example, U.S. Patents 6,326,540 and 6,103,970
- [2] M. S. Tyagi, Introduction to Semiconductor Materials and Devices, (John Wiley & Sons, New York, 1991) pp. 214-235.